



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/686,421

10/15/2003

Yong-Chul Oh

5649-970DV

7289

20792

7590

09/23/2004

MYERS BIGEL SIBLEY & SAJOVEC  
PO BOX 37428  
RALEIGH, NC 27627

EXAMINER

GEBREMARIAM, SAMUEL A

ART UNIT

PAPER NUMBER

2811

DATE MAILED: 09/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

**Application No.**

10/686,421

**Applicant(s)**

OH ET AL.

**Examiner**

Samuel A Gebremariam

**Art Unit**

2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 12-19 and 35-45 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 12-19 is/are allowed.
- 6) ☐ Claim(s) 35-37, 42 and 43 is/are rejected.
- 7) ☒ Claim(s) 38-41, 44 and 45 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- 1) ☐ Certified copies of the priority documents have been received.
  - 2) ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                        | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)               | Paper No(s)/Mail Date. ____.  |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date ____.  | 6) <input type="checkbox"/> Other: ____.                                    |

## DETAILED ACTION

### *Specification*

1. The disclosure is objected to because of the following informalities: page 9, line 20 the "fo" is typographical error. Appropriate correction is required.

### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3. Claim 35 is rejected under 35 U.S.C. 102(e) as being anticipated by Fukaura US patent No. 6,613,645.

Fukaura teaches (figs. 3B–3E) a method for manufacturing a semiconductor device comprising: forming a trench (2) on a semiconductor substrate (1) to define an active region on which devices will be formed; forming a first insulating ( $\text{SiO}_2$ ) layer such that a predetermined thickness of the trench is filled with the first insulating layer; forming selective epitaxial growth (SEG) layers (8, col. 4, lines 39-47) by growing the exposed surface of the active region and the sidewalls of the trench to a predetermined thickness; and filling a space between the SEG layers formed at the sidewall of the trench with a second insulating layer (11). Although the selective epitaxial growth layer is converted to a silicide layer, it was formed as a selective epitaxial layer.

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 36 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fukaura in view of Ho et al. US patent No. 5,747,866.

Regarding claims 36, Fukaura teaches substantially the entire claimed process of claim 35 above except explicitly stating that the process step of forming the trench comprises depositing a pad oxide layer and a mask layer on the semiconductor substrate; patterning predetermined portions of the mask layer and the pad oxide layer; and forming a trench by etching the semiconductor substrate to a predetermined depth using the patterned mask layer and the patterned pad oxide layer as an etching mask. Ho teaches (figs. 1A-1C) the conventional process of forming a trench (shallow trench) by depositing a pad oxide layer (pad SiO<sub>2</sub>) and a mask layer (PAD Si<sub>3</sub>N<sub>4</sub>) on the substrate (Si substrate) and forming the trench by etching the semiconductor substrate to a predetermined depth using the patterned mask layer and the patterned oxide layer as an etch mask.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the trench in the process of Fukaura as taught by Ho in order to form device isolation.

Art Unit: 2811

Regarding claim 37, Fukaura teaches substantially the entire claimed process of claim 35 above including forming a thermal oxide layer at the sidewalls of the trench; and forming a liner (refer to 1C of Ho) on the thermal oxide layer between the step of forming the trench and the step of forming the first insulating layer.

6. Claims 42 and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fukaura in view of Saihara et al. US patent No. 5,963,822.

Regarding claim 42, Fukaura teaches substantially the entire claimed process of claim 35 above except explicitly stating annealing the semiconductor substrate in a hydrogen atmosphere between etching the first insulating layer and forming the SEG layers or between forming the SEG layers and filling the space between the SEG layers formed at the sidewalls of the trench.

Saihara teaches the process of annealing in a hydrogen environment subsequent to forming SEG in order to form a gapless structure between a dielectric layer and SEG film.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the process of annealing in hydrogen environment of SEG layer as taught by Saihara in the process of Fukaura in order to avoid forming a gap between the dielectric and the SEG film.

Regarding claim 43, Fukaura teaches substantially the entire claimed process of claims 35 and 42 above including forming a thermal oxide layer before forming the SEG layer.

***Allowance***

7. Claims 12-19 are allowed.

***Reason for allowance***

8. The following is an examiner's statement of reasons for allowance: The prior art of record does not teach or suggest, singularly or in combination at least the limitation of "forming a first insulating layer in the trench to a height providing an exposed upper portion on opposing sidewalls of the trench; forming a silicon layer on the integrated circuit substrate and extending over an edge of one of the sidewalls of the trench and along at least a portion of the exposed upper portion of the one of the sidewalls" for the method of forming an integrated circuit device.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

***Allowable Subject Matter***

9. Claims 38-41 and 44-45 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Reason for indicating allowable Subject Matter***

10. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record does not teach or suggest, singularly or in combination at least the limitation of "etching the first insulating layer to a predetermined depth such

Art Unit: 2811

that the upper sidewalls of the trench are exposed, wherein in etching the first insulating layer, predetermined portions of the thermal oxide layer and the liner are etched" as recited in claim 38 and "depositing a fluid oxide layer so that the space between the SEG layers is sufficiently filled with the fluid oxide layer; heat-treating the fluid oxide layer so that the density of the fluid oxide layer is improved; and etching back the fluid oxide layer" as recited in claim 44.

### ***Conclusion***


11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References D and E are cited as being related to forming a trench.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel A Gebremariam whose telephone number is (571) 272-1653. The examiner can normally be reached on 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAG  
September 17, 2004



**EDDIE LEE**  
**SUPERVISORY PATENT EXAMINER**  
**TECHNOLOGY CENTER 2800**